Low Read Equivalent Stress Fault Detection in CMOS SRAMs Using MARCH Algorithm

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Abstract

This paper outlines the reduction of Read Equivalent Stress (RES) during test of SRAM memories and demonstrates that the modified pre-charge activity reduces RES because of the predictable addressing sequence. We exploit this observation in order to show minimization of power dissipation during test by eliminating the unnecessary power consumption associated with RES. Read or write operations on a cell involve a stress on the other cells of the same word line is called Read Equivalent Stress. Read Equivalent Stress has the same effect than a read operation. We have calculated 99.8% reduction in RES with the modified pre-charge activity during test for different MARCH algorithms.

Keywords -SRAM, Low Power, Test March, Pre-charge, RES, SoC, dRDF, Functional Mode, Test Mode, Resistive open defect, Addressing sequence.

1. Introduction

Power dissipation during testing of complex Systems-on-Chip (SoC) has been acknowledged as a large portion of power dissipation. The power dissipation during test mode can be several times larger than in normal functional mode [1,2]. In International Technology Road map for semiconductors (ITRS’03) indicated that over 90% of SoC silicon area in 2008 will be employed by memories. Minimizing test power in embedded memories of complex Systems-on-Chip is important since they are becoming the main contributor to the overall SoC silicon area.

When a large number of memories are tested simultaneously, the total power dissipation in the tests can exceed power constraints there by generating excessive heat. Further, it causes potential damage in the devices, yield loss and influences the reliability issues. A direct solution to the power problem is to reduce the number of memories tested in parallel so that the power constraint is valued. However, such solutions impose more test time. Much research has been conducted on power constrained test scheduling. The goal of such scheduling is to maximize the parallelism of memory and other IP core testing without exceeding power limits. The effectiveness of these solutions is limited by the power dissipation of each and every memory and other IP cores during test [3, 4, 5].

In order to reduce memory power dissipation during test, proposals for low power memory BIST have been reported [6, 7]. These proposals all use a gray code address generator instead of binary code in order to minimize signal activities in memory address decoders.

Except for very small memories, however, power dissipation in decoders is often a negligibly small portion of total memory power. In comparison, power dissipation on the memory data path constitutes significant proportion of the total memory power [8, 9].The faults appear as open defects in VDSM technologies. The study indicates the elaboration of the dynamic Read Destructive Faults (dRDFs). According to this work Read equivalent stress (RES) has the similar effect as the read operation. Further, the well known March C- has been modified. This has been done by changing the addressing order for producing a number of RES. More number of RES increases the power dissipation during test [10].
Full functional pre-charge activities are not necessary during test and minimize power dissipation during test by eliminating the unnecessary power consumption associated with the pre-charge activity. This is achieved through a modified pre-charge control circuitry, exploiting the first degree of freedom of March tests. In this work we have analyzed the reduction in RES during testing of different faults in SRAM with different MARCH algorithms for a proposed pre-charge activation model by Dillio Luigi in [11].

2. March Test Solutions

Among the various types Resistive-Open Defects in Core-Cells of test algorithm, March tests allow to reach a good effectiveness with a small complexity. The March test proposed for dRDF detection is generated on the basis of the following requirements[10]:

a. The March elements have to be performed on the memory array with addressing order word line after word line. This is necessary to maximize the number of consecutive RESs, because the RESs are produced only by operating on the core cells of the same row. For example, let us consider the SRAM architecture. The read and write operations of the March elements have to be operated first on all the 512 core-cells of the first word line, then on the 512 core-cells of the second word line, and so on.

b. The elements of the March test have to include w0 operations necessary for sensitization and r0 necessary for observation.

c. Additional elements with w1 and r1 are needed to detect similar faults generated by resistive-open defects placed symmetrically with respect to defect Df4, i.e., in the pull-up of the second inverter composing the core-cell (see Figure 1).

d. All the elements, in particular the sensitization ones, need to be performed in ⇑ and ⇓ addressing order.

In order to justify the last requirement, let us consider the SRAM architecture. If the faulty core-cell is Ci, 0, the first core-cell of the ith row, a March element like ⇑w0 operates a w0 operation on this core-cell and is immediately followed by w0 operations performed on the following 511 core-cells of the same row. These w0 operations imply 511 RESs on the faulty core-cell. If the faulty core-cell is the second one of the row, C, 1, the same March element ⇑w0 involves 510 RESs on the faulty core-cell. In case the defective core-cell is the last of its row, the element ⇓w0 does not involve any RES on the defective core-cell.

![Figure 1: Resistive-open defects injected into the memory core cell](image1)

![Figure 2: Distribution of RESs on a core-cell row with the modified March C cell after the w0 operation. The introduction of a element allows the sensitization phase to be also performed with the opposite addressing order of access on the row. In this condition, the core-cells that endure the maximum number of RESs are those placed in the extremes of the row, while those placed in the middle of the row undergo the smallest number of RESs, i.e., 512/2 = 256 of RESs. In general, if nb_cell is the number of core-cells of each row and nb_op the number of operations (read/write) of the March element (e.g., ⇑w0→nb_op = 1; ⇑r1w0→nb_op = 2), the maximum number of RESs that a core-cell endures is RESmax = (nb_cell − 1) · nb_op and the minimum one is RESmin = (nb_cell · nb_op) / 2 graphically illustrated in Fig. 2, where the name of core-cells is darker when they endure a higher number of RESs.

There are various March tests, which already embed most of the requirements described above and that can be modified with the objective to detect dRDFs. For this purpose, the well-known March C- is considered. This is a 10 N linear test, which is effective to detect stuck-at, transition, and 2-coupling

```plaintext
{⇑ (w0) ⇑ (r0, w1) ⇑ (r1, w0) ⇑ (r0, w0) ⇑ (r0)}
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![Figure 3: March C- structure](image3)
faults and that normally covers 0% of dRDFs. March C- has the structure shown in Figure 3.

The first five elements (M0–M4) could be effective for dRDF sensitization because they contain the w0 or w1 operation. In these elements, the read operations, useful for the observation phase, also contribute to the sensitization phase. Both \( \uparrow \) and \( \downarrow \) addressing orders are operated allowing a good sensitization for all the core-cells. The modification, which makes March C- able to detect dRDFs, consists in the use of the particular address sequence word line after word line. Due to the first of the six degrees of freedom (DOF) of March tests, this modification does not change the capability of March C- to detect the former targeted faults. The efficiency of the modified March C- can be evaluated considering a given SRAM architecture. Let us assume that the defective core-cell is \( Ci, 0 \), the first one of row i. Element M2 operates a w0 on \( Ci, 0 \), and just after the couple of \((r1,w0)\) operations on the following 511 core-cells of the same row i, resulting in \(2 \cdot 511 = 1022\) RESs on the defective core-cell. The same happens if the defective core-cell is \( Ci, 511 \), the last one of row i, and the element M4, which is M2 with inverted addressing order, is operated: on core-cell \( Ci, 511 \), a w0 operation is acted followed by 1022 RESs. Core-cells \( Ci, 0 \) and \( Ci, 511 \) endure the maximum number of RESs because they are placed in the extremes of their row. The core-cells placed in the middle of the row are the less stressed with \( 2 \cdot (512/2) = 512\) RESs. Note that elements M1, as its homologue M3, allows the test of similar faults due to resistive-open defects symmetrically placed with respect to Df4. This modified version of March C- presents many advantages such as its linear complexity and the reuse of an already existing test algorithm.

3. SRAM Test Mode

The addressing order to access the cells and the columns during the memory test mode is predictably known. Therefore, the power dissipation due to pre-charge and RES could be significantly reduced by pre-charge operations in the necessary columns. The addressing sequence has been selected as “word line after word line” for the analysis of the SRAM test mode. If the SRAM is organized as an array of \( n \) rows x \( m \) columns, then read or write operations of each March element need to be operated first on all in cells of the first word line, then on the subsequent \( m \) cells of the second word line, and so on.

During particular addressing sequence, “word line after word line” when one March element is operated on a certain cell of the array, the subsequent cell to be selected, is placed in the column that immediately follows [11]. Thus, the pre-charge action is required in two columns of the memory array for a bit oriented SRAM. The first column is needed for each of the subsequent operation of the current March element due to the restoration of the bit line. The second column is needed as the next cell to be selected is placed there.

In the SRAM test mode, the selected column, pre-charge is OFF during the first half of the cycle and is ON during the second half of the cycle as shown in the Figure 4. In the next column to be selected the pre-charge is turned ON during the entire clock cycle. In the remaining columns the pre-charge circuit can be turned OFF, because the cells of these columns are not involved in the operation.

![Figure 4: Pre-charge action for selected and an unselected column](image)

4. Modified Pre-charge Control Logic

Functional mode and test mode are modes of operation in SRAM. A functional mode in which the memory acts normally and a low power test mode in which the addressing sequence is fixed to ‘word line after word line’ and the pre-charge activity is restricted to two columns for each clock cycle (in bit oriented SRAM) the selected column and the following one(Figure 5). During the final operation on the last cell of each row, the memory returns to functional mode for only one clock cycle to restore the voltage level of all the bit line at VDD. This is necessary in order to prepare the operations in the next row.

A practical implementation of proposed SRAM test model consisting in [11] a modification of the pre-charge control circuitry. The modified pre-charge control logic for model shown in Figure 5 contains an additional element for each column (Figure 6). This element consists of one multiplexer (two transmission gates and one inverter) and one NAND gate. The additional cost of the added logic is ten transistors. The signal LPtest allows write operation. The selection between the functional mode and low power
5. Results & Discussions

When LPtest=1 transmission gate-2 will ON and test mode is selected means of Prj drives the pre-charge of selected cell column and the signal Csj of a selected column j drives the pre-charge of the next column j+1 and all other columns remains OFF (Figure 7). This will reduce RES from 511 to 1(for a 512*512 memory block) when a MARCH element operation in progress on selected cell. For LPtest=0 transmission gate-1 will on and functional mode is selected.

The modified pre-charge logic has little or no effect on the memory performance during normal operation. The switching between the functional mode and the low power test mode is achieved by a multiplexer implemented by two transmission gates (Figure 6). When the functional mode is selected, one of the transmissions gates (on the right of the pre-charge control element, Figure 6) allows signal Prj to drive the pre-charge circuit. We have chosen to use transmission gates (two transistors), instead of a single pass transistor, in order to ensure the minimum delay in the transitions (0→1 and 1→0) of the Prj signal during the normal functional mode, as well as the Csj signal during low power test mode.
6. Conclusion

Modified pre-charge control logic reduces the number of ON pre-charge circuits during the test mode of SRAM. Table 1 shows a comparison between reduction in RES during different March algorithms for full pre-charge activity and modified pre-charge activity. A modified addressing sequence detects new faults and modified pre-charge activity reduces 99.8% RES it results in reduction in power. Different March Algorithms uses different numbers of read or write operations for detecting faults in SRAMs. Reduction in RES is largest in MARCH SR 41n because it uses 41 operations.

Table 1: Reduction in RES with modified pre-charge activity

<table>
<thead>
<tr>
<th>SRAM</th>
<th>MARCH SS22n</th>
<th>MARCH SR 41n</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES(Full pre-charge activity)</td>
<td>2.9470228*10^9</td>
<td>5.4921789*10^9</td>
</tr>
<tr>
<td>RES(Modified pre-charge activity)</td>
<td>5755904</td>
<td>10726912</td>
</tr>
<tr>
<td>Reduction in RES</td>
<td>2.9412669*10^9</td>
<td>5.481452*10^9</td>
</tr>
<tr>
<td>% Reduction in RES</td>
<td>99.8</td>
<td>99.8</td>
</tr>
</tbody>
</table>

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References


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